Indian Institute of Engineering Science and Technology, Shibpur

B. Tech (CS) 5th Semester Mid-Semester Examinations, December 2020

**Microprocessor based design: CS 503**

[Answer should be Machine/Handprinted on the space provided. Drawing should be done separately and imported on the space provided in this question paper. Also, import your signature at the end of the paper. Otherwise, you may write on separate page(s), sign and send the PDF]

Full Marks: 30 Time: 45 Minutes

**Answer the following questions in short**

1. What do you mean by the term n-bit (say, 8, 16 etc.) processor? [2]
2. Suppose that at the end of execution of any instruction the flag register automatically latches the status coming from the logic circuit controlling inputs to the flags. Describe the logic circuit to set/reset Zero flag. [3]
3. What would happen if the CPU data-bus bit 2 is connected to the RAM data-bit 5 and CPU data-bus bit 5 is connected to RAM data bit 2. Assume the rest of the connections are all right – explain. [4]
4. One of the favourable points for I/O mapped I/O available in a typical text is “It is fast” – contradict with proper example. [5]
5. ROM (EPROM) is used as a decoder – advantages and disadvantages [2]
6. When exactly the READY line is checked and what happens if it is found low? [2]
7. Draw the circuit to generate RST 5 that would be supplied to the data bus by the device which has interrupted the CPU through INTR input line, and the CPU acknowledges the request. [3]
8. What happens if the CPU is powered-on with the REDAY line grounded? [2]
9. Use a 74LS156 Dual 2-4 decoder (with open collector output) to activate the \CS lines of the following ICs. [7]

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| --- | --- | --- | --- |
| Sl. No. | Device | SIZE | Address space in the Memory map (starting address only) |
| 1 | EPROM | 8K x 8 | 0000H |
| 2 | RAM1 | 2K x 8 | 2000H |
| 3 | RAM2 | 2K x 8 | 2800H |
| 4 | Input Port | 1 x 8 | 80H |
| 5 | Output Port | 1 x 8 | 80H |

Inputs I0 and I1 are common for both the decoders (A and B). However, you have assorted enable lines; /EA0 and /EA1 for A and /EB0 and EB1 for B.

Signature of the student